AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) An apparatus for generating a region of graphics on a display, the apparatus comprising:

a bus having a first address range and a second address range;

a plurality of registers within said first address range configured to store an X coordinate and a Y coordinate of a pixel to be drawn on said display;

a memory directly connected to said bus and responsive within said second address range;

a calculation circuit configured to calculate an address in said second address range for storage of data corresponding to said pixel in dependence on said X and said Y coordinates; and

a control circuit configured to control writing of said data in said memory ~~at~~ across said bus by driving said address onto said bus.

2. (PREVIOUSLY CANCELLED)

3. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 1, further comprising:

a clipping circuit for (i) comparing said X and said Y coordinates with predetermined clipping limits and (ii) generating a clipping signal configured to indicate that at least one of said X and said Y coordinates falls outside said predetermined clipping limits.

4. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 3, wherein said control circuit is further configured to inhibit writing of said data to said address in response to said clipping signal.

5. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 3, wherein said control circuit is further configured to prevent calculation of said address in response to said clipping signal.

6. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 3, wherein said data is discarded when at least one of said X and said Y coordinates fall outside said predetermined clipping limits.

7. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 1, wherein (i) a first register of said registers is memory mapped to a first location and a second location in said first

address range and (ii) a second register of said registers is memory mapped to a third location and a fourth location in said first memory range.

8. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 7, wherein said apparatus further comprises:

an address decoder for (i) monitoring said first, said second, said third and said fourth memory locations and (ii) applying a location signal to said control circuit representative of an address location being written to.

9. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 8, wherein said control circuit is further configured to control said first and said second registers and said calculation circuit in response to said location signal.

10. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 9, wherein said control circuit is further configured to instruct said calculate circuit to calculate said address in response to one of the following:

said X coordinate being written to a preselected one of said first and said second locations; and

said Y coordinate being written to a preselected one of said third and said fourth locations.

11. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 1, further comprising:

a style table for storing data corresponding to a predetermined pattern for said pixel; and

a style counter for (i) indexing said data in said style table and (ii) generating a style data signal corresponding to said indexed data.

12. (PREVIOUSLY CANCELLED)

13. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 11, wherein said style table is configured to store a non-repeating bit pattern up to a predetermined length for a drawing operation.

14. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 11, wherein (i) a first register of said registers is memory mapped to a first location, a second location, a third location and a fourth location in said first address range and (ii) a second register of said registers is memory mapped to a fifth location, a sixth location, a seventh location and an eighth location in said first address range; and

said apparatus further comprising an address decoder for (i) monitoring said first to said eighth locations, (ii) generating a location signal representative of an address location being written to and (iii) indexing said style counter in response to said address location being written to.

15. (CURRENTLY AMENDED) An apparatus for generating a region of graphics on a display, the apparatus comprising:

a register accessible via a bus for storing coordinates of a pixel to be drawn on said display;

a calculation circuit for calculating an address in a memory directly connected to ~~accessible via~~ said bus for storage of data corresponding to said pixel in response to said coordinates; and

a control circuit for controlling said register and said calculation circuit to cause said data to be stored in said memory across said bus by driving ~~at~~ said address onto said bus, wherein said calculation circuit is configured to output said address in a first part and a second part, said first part comprising a word address corresponding to said address in said memory and representing a single memory word and said second part comprising a bit address representing a position of said pixel data within said single memory word.

16. (CURRENTLY AMENDED) The apparatus as claimed in claim 15, further comprising:

a second register for storing said pixel data in said single memory word prior to said single memory word being written to said address in said memory; and

a ~~multiplexer~~ logic unit for writing data to said second register in dependence on said address calculated by said calculation circuit.

17. (CURRENTLY AMENDED) The apparatus as claimed in claim 16, wherein said ~~multiplexer~~ logic unit combines data for at least two pixels to be drawn in dependence on said address of each of said pixel to permit storage of said data for said pixels in said single memory word.

18. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 17, further comprising:

a comparator connected to said calculation circuit for (i) receiving said addresses, (ii) comparing said addresses of consecutive said pixels to be drawn and (iii) generating a same address signal if said addresses are identical.

19. (PREVIOUSLY AMENDED) The apparatus as claimed in claim 18, wherein said control circuit is further configured to

combine said data for said pixels in response to a receipt of said same address signal.

20. (CURRENTLY AMENDED) A method of generating a region of graphics on a display, the method comprising:

(A) storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

(B) storing a Y coordinate for said pixel in said first address range;

(C) calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates; and

(D) controlling writing of said data across said bus into ~~in~~ a memory directly connected to said bus by driving ~~at~~ said address onto said bus.

21. (PREVIOUSLY AMENDED) The method as claimed in claim 20, further comprising:

comparing said X and said Y coordinates with predetermined clipping limits; and

discarding said pixel data in response to at least one of said X and said Y coordinates exceeding said predetermined clipping limits.

22. (PREVIOUSLY AMENDED) The method as claimed in claim 20, further comprising:

memory mapping a first register storing said X coordinate to a first location and a second location in said first address range; and

memory mapping a second register storing said Y coordinate to a third location and a fourth location in said first address range.

23. (PREVIOUSLY AMENDED) The method as claimed in claim 22, further comprising:

monitoring said first, said second, said third and said fourth locations for a write.

24. (PREVIOUSLY AMENDED) The method as claimed in claim 23, further comprising:

calculating said address for said pixel in response to one of the following:

said X coordinate being written to a preselected one of said first and said second locations; and

said Y coordinate being written to a preselected one of said third and said fourth locations.

25. (PREVIOUSLY AMENDED) The method as claimed in claim 20, further comprising:

storing style data corresponding to a predetermined pattern for said pixel;

indexing said style data; and

generating a style data signal corresponding to said style data as indexed.

26. (PREVIOUSLY AMENDED) The method as claimed in claim 25, further comprising:

selecting a color for said pixel to be drawn in dependence on said style data signal.

27. (PREVIOUSLY AMENDED) The method as claimed in claim 20, further comprising:

storing said data in a single memory word prior to said single memory word being written to said address in said memory in dependence on the word address or a bit address.

28. (PREVIOUSLY AMENDED) The method as claimed in claim 20, further comprising:

combining data for at least two pixels to be drawn in dependence on a word address of each of said pixels to permit storage of said data for said pixels in a single memory word.

29. (PREVIOUSLY AMENDED) The method as claimed in claim 28, further comprising:

comparing said word address of consecutive pixels to be drawn; and

combining said data for said pixels if said word addresses are identical.

30. (CURRENTLY AMENDED) An apparatus for generating a region of graphics on a display, the apparatus comprising:

means for storing an X coordinate for a pixel to be drawn in said region in a first address range of a bus;

means for storing a Y coordinate for said pixel in said first address range;

means for calculating an address in a second address range of said bus for storage of data corresponding to said pixel in dependance on said X and said Y coordinates; and

means for controlling writing of said data <u>across said bus into</u> ~~in~~ a memory <u>directly connected to said bus by driving</u> ~~at~~ said address <u>onto said bus</u>.